Article6

by Author Author

Submission date: 21-Jul-2020 05:11PM (UTC+0530)
Submission ID: 1360363499
File name: 6.docx (428.35K)
Word count: 5597
Character count: 27229

Background

Hearing loss is a debilitating factor for communication breakdown and associated with social isolation. One of the rehabilitative approaches to alleviating hearing loss is hearing aid. With the advancement and proliferation in digital technology, most of its concepts applied in various domain are imbibed and utilized in the fabrication of hearing aid. The budding professionals must have minimal understanding of the working principle of digital hearing aids is an essential part of the knowledge required to troubleshoot the aid. This will help for those who intend to keep up with the knowledge of the digital technology in hearing aid that will inevitably continue. In this mini-review paper, we are presenting the architect of digital hearing aid, the working principle of each component and its limitation are explained with substantial literature review.

The architecture of Digital Hearing Aid

The primary architect of digital hearing aid comprised of arithmetic operations such as ADD, SUBTRACT, MULTIPLY, etc. and logical operation such as AND, OR, NOT, XOR, etc. (Stetzler et al., 2008). The architecture also includes on-chip registers to store immediate results, memories to store signal samples (RAM), and memories to store filter coefficients (ROM). To amplify the discrete version of the signal from the output of the microphone needs multiplication operation. To illustrate, suppose the microphone of the hearing aid picks the signal having 2 volts at one data point, then it converts into binary i.e 010. These binary digits are fed to the digital circuitry to amplify the signal. To be specific, the binary value 010 is multiplied using impulse response, having the characteristics of filter coefficients, which has the application of amplification $10_{(2)}$. The resulting binary value 100, where it accounts for 4 volts (refer convolution section for detailed explanation). Similarly, a series of binary values corresponding to the data point is processed.

To purport, any digital circuit in the hearing aid should fetch (n) binary values from memory corresponding to the input signal plus the program instruction describing what to do with the data to yield accurate results. This digital operation requires a power supply. Stetzler et al., (2008) have developed a digital hearing aid that consumes less power and has thoroughly thrown light on the architecture of the developed hearing aid. The programmable devices are offering more sophisticated algorithms that consume less. Whereas in the analog hearing aid, the components used such as resistors, capacitors, inductors, and transistors are sensitive to environmental changes and subsequent aging deteriorates accuracy of operation. (Philippe et al., 2020)

The Digital Signal Processing illustrated (in **Figure 1**) allows the implementation of sophisticated and complex algorithms in real-time on a Very Large Scale Integrated Chip (VLSI). The VLSI reduces the cost and DSP operations can be easily employed in the digital hearing aid. It can easily be modified in real-time, often by changing in simple programming and or by the reloading of registers in DSP. The same functions may be implemented using hardware, which will pave the way for increasing the speed of the execution, but the circuit complexity will also increase considerably.

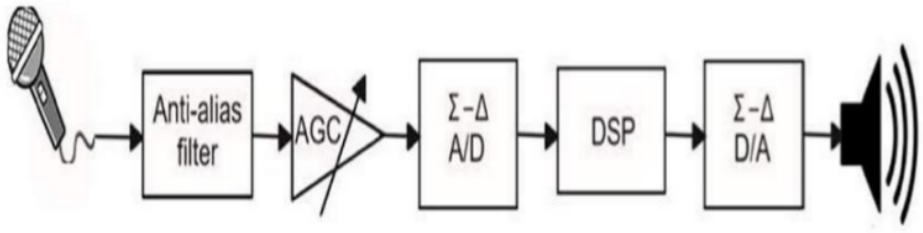


Figure 1. Simplified Block diagram of the architecture of digital hearing aid

A microphone should have the characteristics of a reduced noise floor that transduces the input speech sounds into an electrical representation of acoustic sounds. The electrical signal is passed through a low pass anti-aliasing filter. The audible frequency range for which the human ear responds is 20Hz to 20 kHz, and thereby it is required to remove the frequency content of the input signal beyond 20 kHz. To employ this task, the anti-alias filter that is nothing but low pass filter with cutoff frequency of 20 kHz is employed before the signal transformed to digital signal making use of the A to D converter. This process will remove high-frequency components, thereby preventing aliasing effect, which otherwise increases noise and interference at the output. The resultant output is amplified using an automatic volume control amplifier as the transduced voltage of the input signal picked up by the microphone is too weak. This automatic volume control amplifier is a preamplifier that will increase the mic-level signal to line level signal to support the process of treating the signal in the digital domain after converting the analog signal to a digital signal.

Automatic gain control employs class D amplifier, where the signals are encoded into the duty cycle of the rectangular pulses, which is called pulse width modulation. A high-intensity signal is represented by a high duty cycle, and a low-intensity signal is represented by a low duty cycle. **Figure 2** illustrates the resulting Pulse Width Modulated (PWM) output waveform due to the dynamic nature of the signal, where its intensity varies as a function of time. For example, assume maximum voltage handled by the AGC circuit is 9 volts, and in the following figure, the voltage appears across the circuit for half of the time, which is represented by 50% Duty Cycle. So we can say that effectively it is representing 4.5 volts of the input signal. In the same way, 75% of the Duty cycle represents 6.75 volts of the input signal, and 25% Duty Cycle represents 2.25 volts.

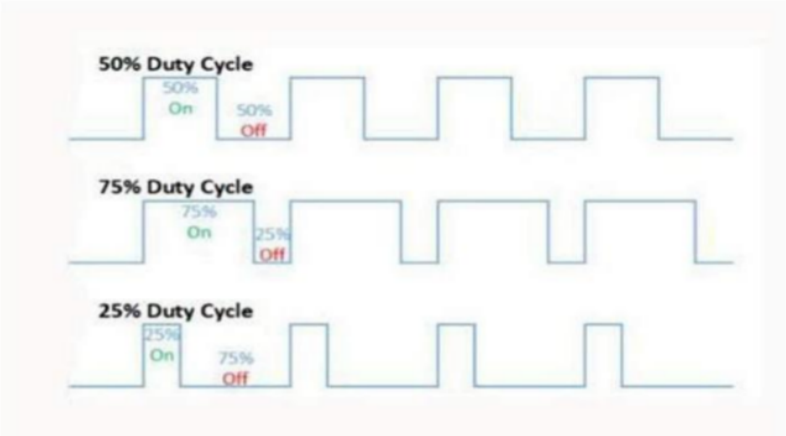


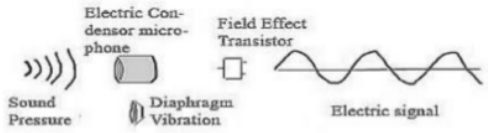
Figure 2. Waveform depicting pulse width modulation depicting the variation of input signal magnitude

The pulse width modulated signal or the rectangular signal is amplified, and then a lowpass filtered, which results in a higher-power version of the original analog signal. Denhardt, (1966) has reported that the utility of Class D amplifiers is increasing due to improvements in higher efficiency in terms of saving power, increased power density, and better audio performance. The output of the Class D amplification employed in the preamplifier is converted from analog signal to digital signal using a sigma-delta analog to digital converter. The operation of sigma-delta modulation is explained in the later section. Once the data is converted to the digital domain, the DSP processes the digital stream using the various algorithms like noise reduction algorithm, frequency shaping algorithm, etc. using a convolution algorithm that makes use of impulse responses. The convolution process using impulse response of the appropriate system could be of filters, equalizers, etc. will help to enhance the speech input. A y [n] represents the output signal obtained from convolving the impulse response (h [n]), with the discrete version of the input signal (x[n]). The desired output is stored in memory. Besides, the output stored may further be modified in terms of increasing the gain as a function of frequency using audio processing algorithms. The sigma-

delta digital to analog converter transforms the digitally processed data back to an electrical signal, which is presented to the real world through the end stage transducer i.e receiver. The detailed description of it is explained in the later section. The electrical signal is converted into an acoustic signal in the end-stage transducer.

Input transducer in the hearing aid. The first and foremost component in the hearing aid is the microphone, which is also called the input transducer converts sound energy into electrical signals. Electret condenser microphone (ECM) technology is most extensively used in all types of hearing aids, whether it could be an analog hearing aid or digital hearing. Electret condenser microphone use fluorocarbon foils as the electret, has uniform frequency response and less variation in sensitivity over temperature (Chakraborty et at, 1975)

,*Figure 3*. Working principle of the electret condenser microphone



One of the plates of the capacitor act as diaphragm vibrates in response to the changes in the air pressure falling on the diaphragm. This results in corresponding variations to the distance between the two plates, that is, the diaphragm and the back plate of the capacitor. This leads to variations in the voltage maintained between the two plates, which is further amplified by using a field-effect transistor. The working principle of electric condenser microphone (ECM) is described in **Figure 3**. The output voltage of the transducer needs to be amplified for improving communication and to decrease the listening effort among the

hearing-impaired population. The technology used to achieve amplification could be either analog or digital. Automatic gain control is a circuit that controls an amplifier's gain in accordance with the instantaneous strength of the input signal picked up by the microphone to maintain a constant output level after amplification. Automatic gain control plays the role of the preamplifier, which is a flexible system in terms of adjusting the gain. This is because the input signal varies above the threshold of AGC in the hearing aids. The adjustment in the gain is a process where the output signal of the AGC is fed back, creating a loop between input and output. This loop will make a way to compare the instantaneous value of the amplitude of the output signal with the set point of error amplifier indicated in figure 4. The output of the error amplifier control the gain of the amplifier in accordance with the feedback signal .If the AGC circuit is installed in the hearing aid, a sufficient amplification is assigned either by reducing or increasing the volume automatically relative to the signal strength.

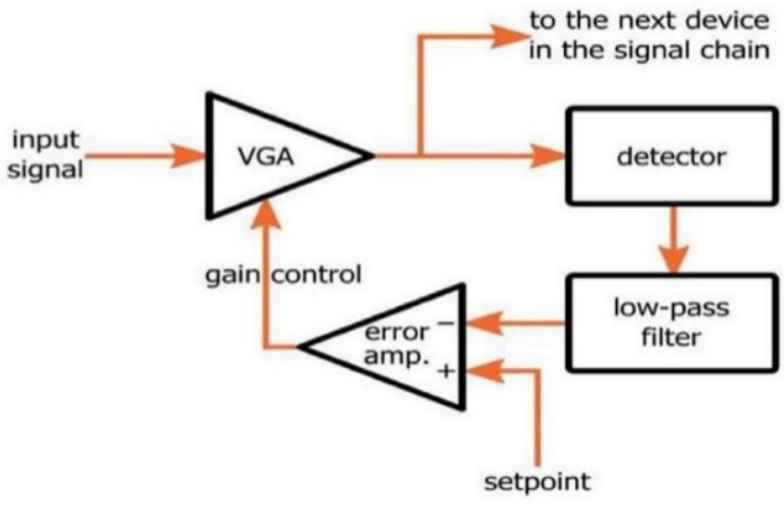


Figure 4. The underlying architecture for an AGC system

The voltage-controlled preamplifier or variable gain preamplifier should be used to step up the low voltage signal picked up by the microphone. Voltage controller detect the speech signal and apply a sufficient gain depending on the applied feedback voltage and it is denoted as control signal (CV). The resultant output voltage of the envelope detector is proportional to the magnitude of the instantaneous input voltage acquired from voltage gain amplifier (VGA). It is assumed that sufficient low pass filtering is applied at its output to reject ripples. The output voltage of the detector is proportional to the envelope of the amplitude of the input signal. In other words, the output voltage of the envelope detector is equivalent to the magnitude of the input voltage. The detector's output is compared against a set point (**Figure-4**) voltage to produce an error signal, which is then integrated to produce a voltage regulated by the gain controller. The control signal is applied to control input of the VGA, which varies the gain depending upon the applied control signal. This control signal is generated based on the difference between the reference signal in the set point and the input signal. If the error voltage is less than the reference voltage, the gain will be increased in VGA to the required voltage for further processing. This technique is usually used in union with feedback loops, leading to their self-correcting mechanism (Keim, 2016)

Analog to digital conversion (ADC). Analog signals are converted into a digital signal. The analog signal has to undergo sampling, quantization, and coding for the conversion process. The different conversion techniques use these processes.

***Successive approximation ADC*.** The signal picked up by the microphone is processed digitally using successive approximation method of ADC. The electrical representation of the speech signal, that is, the transduced output voltage of the microphone is fed into the preamplifier to amplify the signal for further processing. This electrical signal

converted into a discrete signal using an analog to a digital signal converter. The working of two architectures predominately used in the hearing aid, namely the Successive Approximation register ADC and Sigma-Delta ADC, are explained.

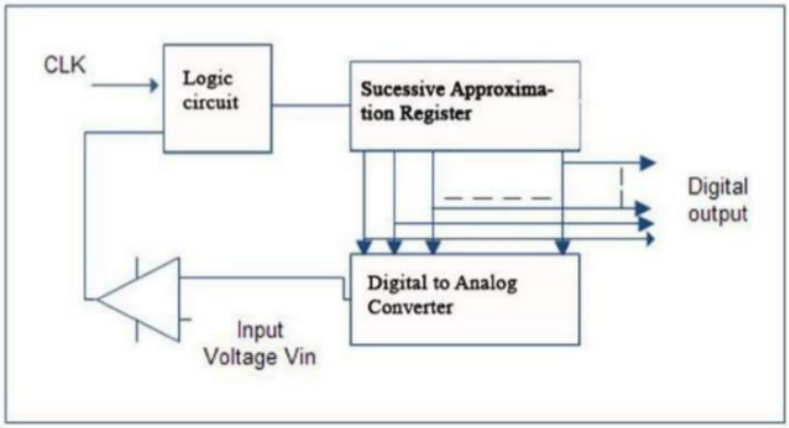


Figure 5. Block schematic representation of successive approximation ADC.

The architecture of successive approximation registor ADC is shown in **Figure 5.** To simplify the illustration, we have considered the 3 bit SAR ADC. The cycle of conversion starts by setting the most significant bit (MSB) of successive approximation registor to '100'. This intermittent digital output (V_d) is converted to an equivalent analog voltage by digital to analog converter and is compared with input sampled voltage (V_i) by making use of comparator, as shown in the block diagram.

This comparison provides an indication by generating a high or low clock pulse through the logic circuit based on the result of the comparison carried out between V_d and V_i. If the result obtained is positive after the process of comparison, it gives an indication that the input sample value is high, enabling the SAR to set the next bit from MSB, which will give rise to binary value '110'. In the same line if the result obtained is negative after the process of comparison, it gives an indication that the input sample value is low lead the SAR to reset

the last set bit and to move on to next bit by setting it high giving rise to binary value '010'. which is. The process continues until digital equivalent of analog input signal value reach the LSB or whichever earlier. The process of conversion can be easily perceived, referring to the flowchart depicted in Figure 6.

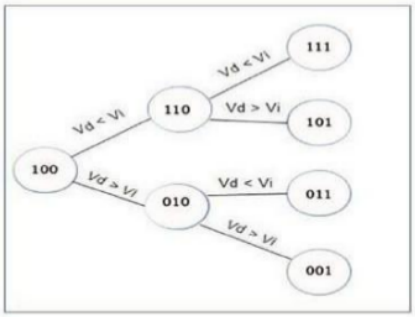


Figure 6 The Flow Chart of successive approximation ADC.

SAR ADCs are known for consuming less power and giving accurate high-resolution output. The foremost limitation of the SAR architecture is that it works with the lower sampling rates and requires an extra circuitry consist of the DAC and the comparator. The complexity involved in designing of SAR ADC is more expensive and relatively takes more time than other ADCs to get the resultant output.

Delta-sigma (DS) analog-to-digital converters (ADCs). The sigma-delta converter makes use of a higher sampling rate, which can also be expressed as N times the Nyquist rate leading to an increase in the sampling rate much greater than sampling frequency. DS ADC converts the analog signal to digital signal with one-bit resolution. **Figure 7** shows the architecture of the sigma-delta ADC. The output signal of the pre-amplifier which acts as an input to DS ADC and is algebraically added (A-E) from the feedback signal fed to into a summing node. The resulting output signal from the summing node is fed to an integrator

(B), and the output of the comparator (C) depends on the integrator's output. The reference voltage is set to -2.5 if the comparator output voltage is negative and vice versa.

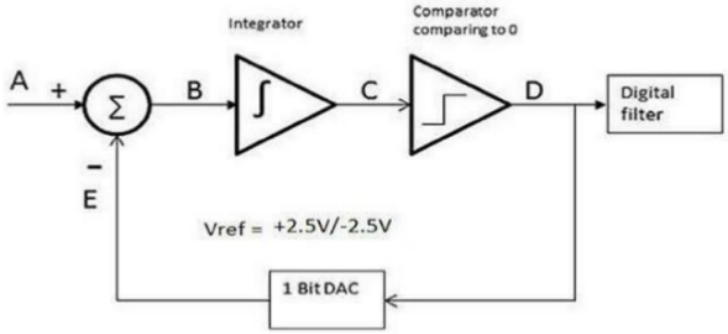


Figure 7. Block diagram of the sigma-delta modulator.

The working can be effectively understood with the following illustration (**Table -1**), the input voltage to the converter from the preamplifier of the hearing aid is 1 V, and the Digital to Analog Converters Voltage Refs are ±2.5 V (+2.5 = High (H); -2.5 = Low (L)). The full-scale measure of sigma Delta ADC is 5 V (i.e. 2.5 – (–2 .5)). Initially, the summing node and integrator voltage are set to 1. If the input voltage of 1 V is fed into summing node, where the reference voltage of 2.5 is subtracted from the input voltage results to -1.5 V. The output of summing node is algebraically summed with the initial setting of integrator voltage of 1 V. The resultant voltage in the integrator is -0.5 V where it compares with the digital reference in the comparator. Since the output is in negative voltage, the DAC is set at low, that is -2.5. In the successive cycle, the value of DAC (-2.5 V) is subtracted with the input voltage in the summing node. The resultant output is 3.5 V, which is algebraically added with the previous voltage in the integrator (-0.5 V) results to 3 V. If the voltage in the integrator is positive, the digital reference turns out to be high (that is + 2.5 V). Likewise, the process iterates until we

get the digital output closer to the input voltage. In the table, we can see that there are six times digital reference set to high (+2.5) and two times set to low (-2.5). Averaging the number of times, the digital reference has set to high by the total number of iteration should closely match the input voltage (6/8 =0.75) if the iteration is more, than obviously, the digital output will be precise to the input voltage. The high is considered as 1 in binary digit and low as 0 in the binary digit. In this illustration, 1 volt of input is coded as HLHHHLHH or 10111011.

Here Table-1

The output of the difference amplifier equals the input plus the quantization noise. By algebraically summing the error voltage with the input signal, the accuracy of conversion is increased by reducing the quantization noise. The integrator performs low-pass filter action on to the input signal and a high-pass filter action to the quantization noise leading to push the quantization noise to higher frequencies, as shown in **Figure 8a. Figure 8b and 8c** determine the sampling frequency. The above process will lessen the quantization noise in the Sigma Delta ADC.

Conversely, if this process is not employed then the quantization noise is uniformly distributed over the entire frequency band distorting the frequency of interest. Nevertheless, in the sigma-delta ADC, the distortion is kept to a minimum as the negative feedback loop minimizes the quantization noise making the integrator to shape noise distribution such that the quantization noise is decreased in the low-frequency band and increased in the high-frequency band. This process is called **noise shaping.** The function of the comparator is to compare a reference voltage with the output of the integrator to generate the output as “high” or “low” depending on the output of the comparator. The Digital to Analog Converter uses the output of the Analog to Digital Computer and generates reference voltages depicted in

Table 1. The feedback loop feeds back this reference voltage to the summing node where the reference voltage is algebraically added with the input signal again. These feedback cycles bring the DAC's output to be the average of the input signal.

Suppose if the signal has the highest frequency of 8 kHz, then sampling frequency should be twice the highest frequency, that is, the sampling frequency should be at least 16 kHz to avoid aliasing. In such a case, the quantized noise will be accumulated in the signal of interest (**Figure-8a**) (Loloee, 2020; Rietjens et al., 2011). To reduce the quantization error, it is ideal to increase the sampling rate and the number of bits (2^n) such that the sampled point is mapped to the nearest quantization level such that quantization error referred as noise reduces after low pass filtering (**Figure-8b**). The oversampling frequency utilized in the SDM eliminates the noise. The error in the signal (A-E) is partial out in the summing node. The output from the summing node is algebraically summed in the integrator results in the reduction of noise as a function of successive iterations. In SDM, the integrator acts as a low pass filter, and this process is called noise shaping (**Figure 8c**). The decimator in the sigma-delta demodulator reduces the sampling frequency for subsequent ease of processing of digits to convert back into the analog signal.

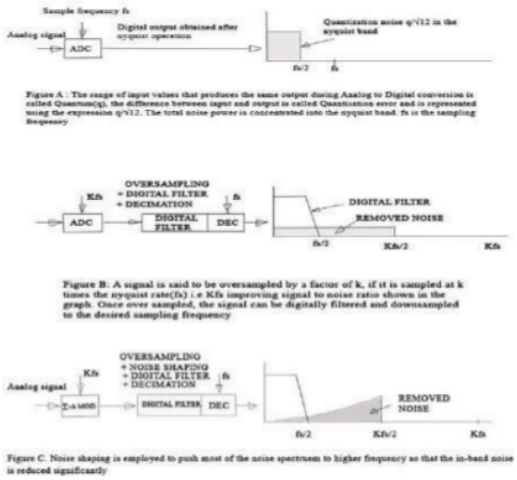


Figure A : The range of input values that produces the same output during Analog to Digital conversion is called Quantum(q), the difference between input and output is called Quantization error and is represented using the expression $q^2/12$. The total noise power is concentrated into the nyquist band. fs is the sampling frequency

Figure B: A signal is said to be oversampled by a factor of k, if it is sampled at k times the nyquist rate(fs) i.e Kfs improving signal to noise ratio shown in the graph. Once over sampled, the signal can be digitally filtered and downsampled to the desired sampling frequency

Figure C: Noise shaping is employed to push most of the noise spectrum to higher frequency so that the in-band noise is reduced significantly

Figure 8. The technique of oversampling with an analysis in the frequency domain.

Processing of digitized signal. Once the signal is digitalized in the ADC circuit, the output is processed using impulse response. One of the digital signal processing techniques used is convolution, which is a mathematical operation of two functions, where the input digitalized signal x[n] is modified according to the function h[n], thereby the desired digitized output is emanated y[n]. Convolution operation can be carried out in time domain as well as in the frequency domain. The following discussion explains convolution in the time domain

Convolution method of the impulse response. Convolution is the digital signal processing technique wherein the two signals are combined using a mathematical technique or convolution algorithm, which involves multiplication and addition. Convolution is a fundamental and vital concept in signal processing and analysis and it is represented by the asterisk symbol (*). To carry out the process of convolution, we require two signals as input to yield the third signal, which can be treated as the digitally processed output signal. Among the two input signals, the first signal is the impulse response of the system, which is also

called as filter kernel or convolution kernel, and the second input signal is any arbitrary input signal which is processed based on the type of kernel utilized in the convolution algorithm. Impulse response determines the output of the system for any arbitrary signal. (John Santiago, 2020 ; Winograd, 1980). The underlying working is depicted in the following block diagram (**Figure-9**).

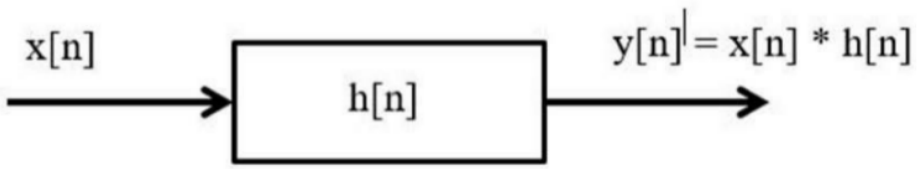


Figure 9. Pictorial representation of convolution operation in the Time domain. X[n] represents the discrete version of the input signal, h[n] is the impulse response, and y[n] is the output signal.

To illustrate the process of convolution we have considered arbitrary input x[n] = {2,4,6,4,2} and the impulse response of the amplifier system represented by h[n] = {3,-1,2,1}. The following steps are to be followed to implement the convolution algorithm, which lead to the results represented in **Table 2**.

The steps are listed as follows:

1. First, decompose the discrete-time index n to i in the input signals x[n], and impulse response h[n] as represented in Figure 10 wherein each sample can be treated individually.

2. The input signals x[i] is flipped left for the right to obtain x[-i] as represented in Figure 3.

3. Shift the input signal by x[n-i] to get each output index n

4. The convolution x[n]*h[n] is performed and y[n] is computed by synthesizing the values of x[n-i]*h[i] as i ranges over the set of integers.

Here Table-2

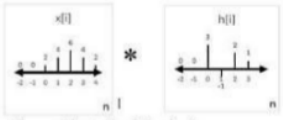


Figure a: Discrete-time index signals.

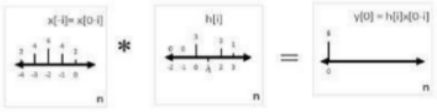


Figure b: First Iteration of the convolution process and the value of n=0.

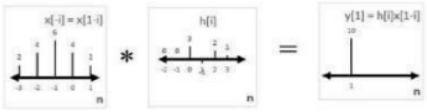


Figure c: Second Iteration of the convolution process and the value of n=1

Figure 10. A. Discrete-time index n to i in the signals x[n] and h[n] and B-C represents the iteration of the convolution process.

The illustration of convolution method is explained in Figure-8. Now we flip x[i] in order to obtain x[-i]. For n = 0, there will be no shift x[0-i] = x[-i]. For n = 0, the of product x[n-i]*h[i] is determined and then added up to get the discrete y[0]. To illiterate [h[0] =3*x[0]=2 then the y[0] =6; h[-1]=0*x[-1]=4 then the y[0] =0; h[-2]=0*x[-2]=6 then the y[0]=0, then the product of all iteration should be added to obtain ∑y[0] i.e., 6+0+0 = 6]. For n = 1, there will be right shift of x[1-i] by 1 unit, then the product of x[1-i]*h[i] are added up to obtain y[1]. Likewise, the above process is repeated for n corresponding to 2,3 4,5,6 and 7

to obtain y[n], which is the resultant amplified version of the arbitrary input signal (**Figure-11**).

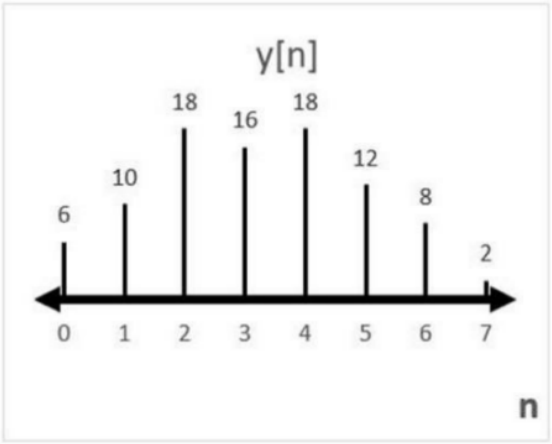


Figure 11. Pictorial representation of y[n] obtained after convolution as per the data considered in our illustration

Restoring the processed digitized data back to analog. The output of Delta sigma (ΔΣ) DAC is represented as an assembly of pulses, which can also be called as bitstream. These pulses are allowed to pass through a low-pass filter to remove the noise inserted during the conversion process, which increases the precision of the analog output voltage, as depicted in **Figure 12**. The resolution of a DAC determines the minute change in the analog voltage (that is the minimum change in the analog voltage that causes the output of the DAC to change) specified by the number of input bits or input width, The Full-scale (Fs) determines the output span which represents the output when all the input bits are assigned ones subtracted from the output when all the input bits are assigned to zeroes. Full-scale is represented by the number of voltage levels (2^N for an N-bit DAC) that can be produced by the Digital to Analog Converter. A DAC is employed to signify the voltages from zero volts to the maximum power-supply voltage, V_{CC}. The lowest DAC input code should depict 0 V,

and the highest input code should depict $V_{CC,}$ which represents the full-scale voltage. Each input analog voltage stage of an N-bit Digital to Analog converter is given by (Cheung et al., 2005)

$$V_{LSB}= \frac{F_S}{2^N}$$

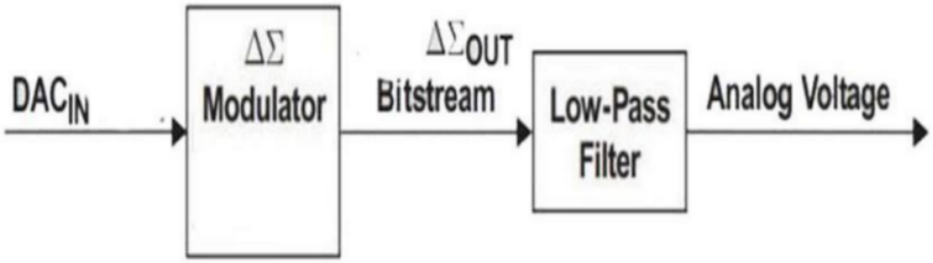


Figure 12. Block diagram of Sigma Delta DAC

The analog output of the filter is an analog voltage, which is equivalent to the average of the on-time of the pulses fed to the input to the low-pass filter. The frame period has to be distributed into 2^N parts. The on-time is characterized as one within the stream of bits in the frame. The analog voltage is given by the formula mentioned below.

$$\frac{On-time}{2^N} \times FS$$

For example, **in Figure 13,** explains the DAC for the average analog output equals to 3/8 × V_{CC}.

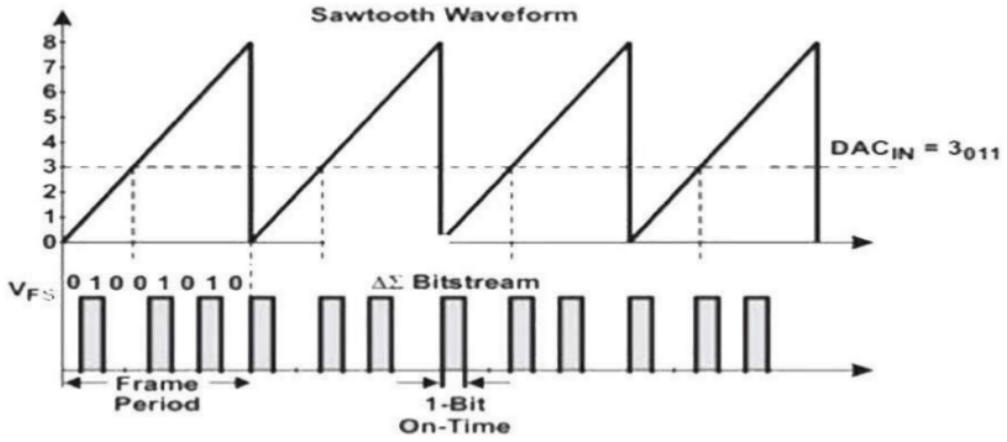


Figure 13. Bit stream output of Sigma Delta DAC for D_{IN} 3_{011}

In this process, the output is a pool of pulses of equal width such that the average density of the pulses corresponds to the digital input value. These pulses or the output stream representing the digital output is fed through a low-pass filter to produce equivalent analog voltage. The ΔΣ operation is explained with a 3-bit example in Table -3. Let us consider Fs =6 V, 8-bit stream in a frame and number of on-time pulses within the frame is 4 (10101010) then the output voltage delivered is 5.3 V. **Table 3** shows the stream of bits representing the inputs of a 3-bit DAC and their equivalent average analog output voltage.

Here Table-3

Output transducer of the hearing aid. The receiver gathers electrical signals from the DAC and converts them back into acoustic energy. Balanced armature receivers (BAR) are the preferred technology in the application of receiver by considering the efficiency (battery life) and size. It offers superior sound output and cleaner midrange sound compared to similar-size dynamic style receivers. It provides up to 20% space savings versus similar competitive types and up to 75% versus dynamic receivers. Efficiently transforms electrical energy representing the processed input signal into sound waves or acoustic energy. The power consumed by BAR is very low eventually saving the battery life of the hearing aid.

The Balanced armature technology's transduction principle transduces the electrical signal to acoustic signal covering even higher frequency range. BAR is cost-effective as the design is very simple and consumes less space which helps in miniaturized the hearing aids.

Balanced Armature (BA) transducers work based on the electromagnetic principle (**Figure 14**) and exhibit deliberately sophisticated efficiency when compared to electro-dynamic transducers. The permanent magnets generate a magnetic field in which the armature is balanced. When the coil is subjected to the flow of electric current a magnetic flux is induced in the armature. It eventually results the end of the armature to be attracted to either of the poles of the permanent magnets. The oscillations of alternating electric current cause the armature to bend and moves up and down. The movement to the diaphragm is initiated by the movement caused by the driver pin to which armature is connected. As the diaphragm moves upwards and downwards the surrounded air molecules compresses and magnifies leading to the creation of the sound wave (Dagastine, 2018). BAR receivers are linear, time-invariant and stable in delivering the accurate output.

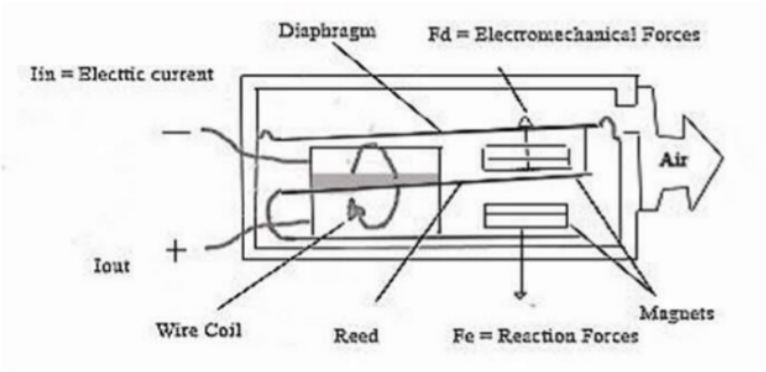


Figure 14. The schematic diagram of Balanced Armature transducers with diaphragm controlled electromagnetically in order to generate sound.

Conclusion

There has been much exaggeration connected with technicality behind the functioning of digital Hearing aid. This article can support the hearing health professional to unveil the technology behind working and functioning of digital hearing aid in terms of providing insight about how analog signal available in nature is converted to discrete signal and then back to the analog signal.

Conflict of Interest: No conflict of interest

Source of Funding: None.

Acknowledgment: We thank The Director and Principal of JSSISH, Mysuru, for permitting to take up this work.

References

Chakraborty, P. K., Kapoor, M. R., & Pavate, K. D. (1975). Electret Condenser Microphone. *J Inst Electron Telecommun Eng*, *21*(7), 383–385. https://doi.org/10.1080/03772063.1975.11450752

Cheung, B. H., Acquisition, D., & Email, P. (2005). *Implementation of 12-bit delta-sigma DAC with MSC12xx controller*.

Dagastine, G. (2018). On the cutting edge of hearing aid research. *Mechanical Engineering*, *140*(1), 30–32.

Denhardt, D. T. (1966). A membrane-filter technique for the detection of complementary DNA. *Biochemical and Biophysical Research Communications*, *23*(5), 641–646. https://doi.org/10.1016/0006-291X(66)90447-5

John Santiago. (2020). *Apply the Impulse Function to Circuit Analysis*.

Keim, R. (2016). Understanding Automatic Gain Control. In *All About Circuits*.

Loloee, A. (2020). *Understanding Delta-Sigma Modulators*. 1–19.

Philippe et.al. (2020). *Analogue Processing*. 1–11.

Rietjens, I. M. C. M., Louisse, J., & Punt, A. (2011). Tutorial on physiologically based kinetic modeling in molecular nutrition and food research. *Molecular Nutrition and Food Research*, *55*(6), 941–956. https://doi.org/10.1002/mnfr.201000655

Stetzler, T., Magotra, N., Gelabert, P., Kasthuri, P., & Bangalore, S. (2008). *Low power real-time programmable DSP development platform for digital hearing aids*. *April*, 2339–2342 vol.4. https://doi.org/10.1109/icassp.1999.758407

Winograd, S. (1980). 5. FIR Filters. *Arithmetic Complexity of Computations*, 39–56. https://doi.org/10.1137/1.9781611970364.ch5

Figure legends

SL.No	Legend of the Figure
1	Simplified Block diagram of the architecture of digital Hearing Aid
2	Waveform depicting pulse width modulation depicting the variation of input signal magnitude
3	Working principle of the electret condenser microphone
4	Underlying architecture for an AGC system
5	Block schematic representation of successive approximation ADC.
6	The Flow Chart of successive approximation ADC.
7	Block diagram of sigma delta modulator.
8	Technique of oversampling with an analysis in the frequency domain.
9	Pictorial representation of convolution operation in Time domain
10	Discrete-time index n to i in the signals x[n] and h[n] and B- C represents the iteration of convolution process.
11	Pictorial representation of y[n] obtained after convolution as per the data considered in our illustration
12	Block diagram of Sigma Delta DAC
13	Bitstream output of Sigma Delta DAC for DIN 3011
14	The schematic diagram of Balanced Armature transducers with diaphragm controlled electromagnetically in order to generate sound.

Table 1

The voltages are calculated and passed around within the modulator to create the resulting bitstream

VOLTAGE CALCULATIONS				
Vin = 1	Summing node	Integrator V_o	Comparator	DAC
	1	1	H	2.5
	1-(2.5) = -1.5	1+(-1.5) = -0.5	L	-2.5
	1-(-2.5) = 3.5	(-0.5)+3.5 = 3	H	2.5
	1-(2.5) = -1.5	3 + (-1.5) = 1.5	H	2.5
	1-(2.5) = -1.5	1.5+(-1.5) = 0	H	2.5
	1-(2.5) = -1.5	0 +(-1.5) = -1.5	L	-2.5
	1-(-2.5) = 3.5	(-1.5)+3.5 = 2	H	2.5
	1-(2.5)= -1.5	2+(-1.5) = 0.5	H	2.5

Table 2

Process of Convolution using the Text Table Method

n	n<0	0	n-1	n-2	n-3	n-4	n-5	n-6	n-7	n>7
x[n]	0	2	4	6	4	2	0	0	0	0
h[n]	0	3	-1	2	1					
h[0]x[n]	0	6	12	18	12	6	0	0	0	0
h[1]x[n-1]	-	-	-2	-4	-6	-4	-2	0	0	0
h[2]x[n-2]	-	-	-	4	8	12	8	4	0	0
h[3]x[n-3]	-	-	-	-	2	4	6	4	2	0
y[n]	0	6	10	18	16	18	12	8	2	0

Table 3

Bitstream and average analog output voltage for 3-bit DAC inputs

DAC_{IN}	DAC_{OUT} BITSTREAM	ANALOG OUTPUT VOLTAGE (FS = V_{CC}) (V)
0_{000}	00000000	0
1_{001}	00000010	$\frac{1}{8}$ *X Fs*
2_{010}	00100010	$\frac{2}{8}$ *X Fs*
3_{011}	01001010	$\frac{3}{8}$ *X Fs*
4_{100}	10101010	$\frac{4}{8}$ *X Fs*
5_{101}	10110110	$\frac{5}{8}$ *X Fs*
6_{110}	11101110	$\frac{6}{8}$ *X Fs*
7_{111}	11111110	$\frac{7}{8}$ *X Fs*
8_{1000}	11111111	*Fs*

Article6

ORIGINALITY REPORT

12%	7%	1%	8%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	focus.ti.com Internet Source	3%
2	Submitted to University of Southampton Student Paper	1%
3	Submitted to National Institute of Technology Karnataka Surathkal Student Paper	1%
4	mafiadoc.com Internet Source	1%
5	www.freepatentsonline.com Internet Source	1%
6	www.ti.com Internet Source	<1%
7	lib.dr.iastate.edu Internet Source	<1%
8	Submitted to The University of the South Pacific Student Paper	<1%
9	Submitted to University of East London	

	Student Paper	<1%
10	Submitted to Leiden University Student Paper	<1%
11	Submitted to 8779 Student Paper	<1%
12	Submitted to University of Leeds Student Paper	<1%
13	Submitted to University of Auckland Student Paper	<1%
14	Submitted to Brigidine College St Ives Student Paper	<1%
15	Submitted to University of Bradford Student Paper	<1%
16	Submitted to Anna University Student Paper	<1%
17	www.clear.rice.edu Internet Source	<1%
18	dsppc14.csie.nctu.edu.tw Internet Source	<1%
19	Submitted to American University of Beirut Student Paper	<1%
20	Whitley, Julie Anne, and Bonnie L. Rich. "A	<1%

	Double-Blind Randomized Controlled Pilot Trial Examining the Safety and Efficacy of Therapeutic Touch in Premature Infants :", Advances in Neonatal Care, 2008. Publication	
21	Submitted to University of Macau Student Paper	<1%
22	ris.uni-paderborn.de Internet Source	<1%
23	Submitted to University of Salford Student Paper	<1%
24	Submitted to Sheffield Hallam University Student Paper	<1%
25	Submitted to Nanyang Technological University, Singapore Student Paper	<1%
26	F. Parhizgar, Reza Asgari, Saeed H. Abedinpour, M. Zareyan. "Anisotropic RKKY interaction in spin-polarized graphene", Physical Review B, 2013 Publication	<1%
27	Submitted to University of Westminster Student Paper	<1%
28	Submitted to Taibah University Student Paper	<1%

Exclude quotes	On	Exclude matches	Off
Exclude bibliography	On		